



Europäisches Patentamt
European Patent Office
Office européen des brevets



Publication number:

0 567 016 A2

EUROPEAN PATENT APPLICATION

Application number: 93106238.4

Int. Cl.⁵ H05K 3/46

Date of filing: 16.04.93

Priority: 20.04.92 JP 99427/92
20.04.92 JP 99579/92
04.02.93 JP 17517/93

Date of publication of application:
27.10.93 Bulletin 93/43

Designated Contracting States:
DE FR GB

Applicant: Sumitomo Electric Industries, Ltd.
5-33, Kitahama 4-chome, Chuo-ku
Osaka 541(JP)

Inventor: Hattori, Hisao, c/o Itami Works of
Sumitomo Elec.
Ind. Ltd.,
1-1, Koyakita 1-chome
Itami-shi, Hyogo(JP)
Inventor: Yoshino, Hiroshi, c/o Itami Works of
Sumitomo Elec

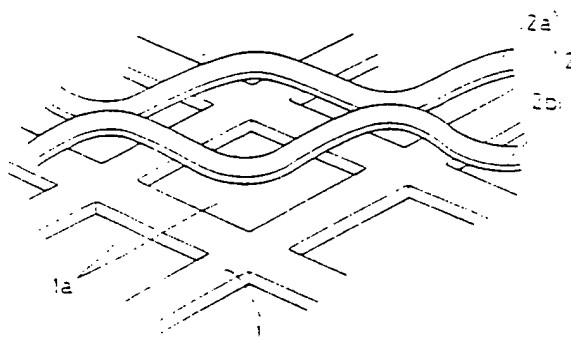
Ind. Ltd.,
1-1, Koyakita 1-chome
Itami-shi, Hyogo(JP)
Inventor: Ihara, Tomohiko, c/o Itami Works of
Sumitomo Elec
Ind. Ltd.,
1-1, Koyakita 1-chome
Itami-shi, Hyogo(JP)
Inventor: Yamanaka, Shosaku, c/o Itami
Works Sumitomo Elec.
Ind. Ltd.,
1-1, Koyakita 1-chome
Itami-shi, Hyogo(JP)

Representative: Schieschke, Klaus, Dipl.-Ing.
Patentanwälte Dipl.-Ing. E. Eder
Dipl.-Ing. K. Schieschke
Elisabethstrasse 34
D-80796 München (DE)

Multi layered wiring board and method for manufacturing the same.

A multilayered wiring board having a multilayered wiring structure. A first meshed wiring layer having a plurality of holes formed therein and a second wiring layer having a plurality of wirings are provided. The wirings of the second wiring layer wind up and down so as to partially sink in the holes formed in the first wiring layer. In another arrangement, the first wiring layer has a plurality of protrusions protruding into spaces between the adjacent ones of the wirings of the second wiring layer. The crosstalks between the wirings are reduced.

FIG. 1



With the method of manufacturing a multilayered wiring layer according to the first embodiment, an insulating layer is formed on the meshed first wiring layer. Recesses are formed in the insulating layer at portions right over the holes in the first wiring layer. Thus, the wirings of the second wiring layer are bent along the recesses formed in the insulating layer and sink in the holes of the first wiring layer.

With the multilayered wiring board of the second embodiment, the protrusions formed on the first wiring layer extend into the spaces defined between the adjacent wirings of the second wiring layer. This increases the electrostatic coupling between the wirings of the second wiring layer and the first wiring layer. Namely, the electrostatic coupling therebetween is greater than the electrostatic coupling between the respective wirings of the second wiring layer. Thus, crosstalks between the respective wirings of the second wiring layer can be reduced to a low level.

With the manufacturing method of the second embodiment, a plurality of protrusions are formed on the meshed first wiring layer and an insulating layer is formed on the first wiring layer. A second wiring layer comprising a plurality of wirings is further laminated on the insulating layer so that the wirings extend between the protrusions of the first wiring layer. The protrusions of the first wiring layer protrude into the spaces between the wirings of the second wiring layer.

With the manufacturing method of the third embodiment, the first wiring layer is formed on a protrusion-formed layer having a plurality of protrusions. Protrusions are thus formed on the first wiring layer at portions right over the protrusions of the protrusion-formed layer. An insulating layer is provided on the first wiring layer. A second wiring layer comprising a plurality of wirings is formed on the insulating layer so that the wirings extend between the protrusions of the first wiring layer. Namely, the protrusions of the first wiring layer protrude into the spaces between the wirings of the second wiring layer.

Other features and objects of the present invention will become apparent from the following description made with reference to the accompanying drawings, in which:

Fig. 1 is an enlarged perspective view of a portion of one embodiment of the multilayered wiring board according to the present invention;

Fig. 2 is a top plan view of the multilayered wiring board of Fig. 1;

Fig. 3 is a sectional view of the multilayered wiring board of Fig. 1;

Fig. 4 is a view illustrating one embodiment of the manufacturing method according to the present invention;

Fig. 5 is an enlarged perspective view of a portion of a conventional multilayered wiring board;

Fig. 6 is a sectional view of the wiring board of Fig. 5;

Fig. 7 is an enlarged perspective view of a portion of another embodiment of the multilayered wiring board according to the present invention;

Fig. 8 is a top plan view of the wiring board of Fig. 7;

Fig. 9 is a sectional view of the wiring board of Fig. 7;

Fig. 10 is a view illustrating another embodiment of the manufacturing method according to the present invention;

Fig. 11 is a sectional view of a further embodiment of the multilayered wiring board; and

Fig. 12 is a view illustrating a further embodiment of the manufacturing method according to the present invention.

First, description will be made of the embodiments of the multilayered wiring board according to the present invention.

Fig. 1 is an enlarged perspective view of a portion of one embodiment. The multilayered wiring board has a first wiring layer 1 and a second wiring layer 2 which are laminated over the first layer through an insulating layer (not shown). The first wiring layer 1 is mesh-shaped and has numerous holes 1a. The second wiring layer 2 comprise wirings 2a and 2b which are meandering up and down so as to sink partially into the holes 1a formed in the first wiring layer 1.

Fig. 2 is a top plan view of the multilayered wiring board of this embodiment. As is apparent from this figure, the holes 1a formed in the first wiring layer 1 are square in shape and arranged regularly in a plurality of rows. The wiring 2a extends along the diagonal lines of the holes 1a arranged in a single row. The wiring 2b extends along the diagonal lines of the holes 1a in the next row. Thus, the distance or pitch between the axes of the wirings 2a and 2b is substantially equal to half the length of the diagonal line of each hole. For example, if the diagonal line of each hole 1a is 100 microns, the pitch of the wirings 2a and 2b will be 50 microns. If the pitch is 50 microns, the width of each of the wirings 2a and 2b are set to be 25 microns, which means that the space between wirings are also 25 microns. These wirings 2a and 2b sink in all the holes 1a one after another.

Fig. 3A shows a section taken along line A-B of Fig. 2. Fig. 3B does a section taken along line C-D of Fig. 2, and Fig. 3C is a section taken along line E-F.

As shown in these figures, the first wiring layer 1 is formed on a board 3. An insulating layer 4 is

also formed on the board so as to cover the wiring layer 1. The insulating layer 4 is recessed right over the holes 1a in the first wiring layer 1. Since the wirings 2a and 2b are provided to overlie the insulating layer 4, they also sink at portions right over the holes 1a in the first wiring layer 1.

Thus, the distance between the wirings 2a and 2b and the first wiring layer 1 is short at these portions, so that the electrostatic couplings between the wiring 2a and the first wiring layer 1 and between the wiring 2b and the first wiring layer 1 are strong at these portions. With this arrangement, if the mesh-shaped first wiring layer 1 is grounded while using the wirings 2a and 2b as signal transmission lines, crosstalks between the wirings 2a and 2b can be kept at a low level. Also, since the holes 1a are arranged in a staggered manner, the wiring 2a and 2b are corrugated up and down so that when the one wiring 2a sinks into the hole 1a, the other wiring 2b remains above the hole, and vice versa. With this arrangement, the distance between the wirings 2a and 2b can be kept large. Thus, crosstalks between the wirings 2a and 2b can be reduced still further.

Preferably, the second wiring layer 2 should sink in the holes 1a in the first wiring layer 1 by the amount within the range of 1 - 5 microns. If less than 1 micron, crosstalks cannot be suppressed sufficiently. If larger than 5 microns, it is difficult to form the second wiring layer 2 with high dimensional accuracy.

Fig. 5 shows a conventional multilayered wiring board, in which straight wirings 102a and 102b are provided on the top of a meshed wiring layer 101 through an insulating layer (not shown). Figs. 6A, 6B and 6C are sectional views of this wiring board, each corresponding to Figs. 3A, 3B and 3C, respectively. As will be apparent from these figures, compared with the embodiment, the wirings 102a and 102b are rather spaced apart from the meshed wiring layer 101 and the distance between the wirings 102a and 102b is short. Crosstalks between the wirings 102a and 102b are thus high.

Next, referring to Fig. 4, we shall describe a method of manufacturing the multilayered wiring board according to the first invention shown in Figs. 1 - 3.

First, we will describe the first embodiment of the manufacturing method.

(step a)

The surface of a board 3 made of Al_2O_3 is polished to provide a mirror finish

(step b)

A metal film is formed by deposition on the board 3 to form the first wiring layer 1. The metal film has a three-layer structure comprising a 0.1-micron thick Cr film, a 5-micron thick Cu film and a 0.1-micron thick Cr film laminated one on another so that the total thickness will be about 5 microns.

(step c)

A resist pattern 11 that represents the mesh pattern is formed on the first wiring layer 1 by photolithography.

(step d)

The Cr and Cu films of the metal films forming the first wiring layer 1 are subjected to wet etching using red prussiate and ferric chloride etching solutions to form the first wiring layer 1 into mesh shape.

(step e)

The resist pattern 11 is stripped off

(step f)

A photosensitive polyimide varnish containing 17.5% of resinous component is applied to the surface of the first wiring layer 1. Since the content of resinous component in the polyimide varnish is low, it will be depressed, when hardened later, at portions right over the holes 1a formed in the first wiring layer 1, thus forming an insulating layer 4 having a plurality of recesses.

(step g)

The photosensitive polyimide varnish is exposed to light, developed and cured to form a 10-micron thick insulating layer 4. The conditions are adjusted to have recesses about 2 microns deep. The insulating layer 4 is also formed with via holes 12.

(step h)

A metal film is deposited on the insulating layer 4 by sputter-deposition to form a second wiring layer 2.

(step i)

A resist pattern 13 that represents a wiring pattern is formed on the second wiring layer 2 by

second wiring layer 2 are connected together through the via holes 12. The connection through the via holes 12 is not illustrated in Figs. 1 - 3.

(step j)

The second wiring layer 2 is subjected to wet etching to shape the second wiring layer 2 into a predetermined pattern. Then the resist pattern 13 is stripped off.

The above-mentioned manufacturing steps were controlled so that each hole 1a formed in the first wiring layer 1 had a diagonal length of 100 microns, the width of each wiring 2a and 2b and the gap therebetween are 25 microns and the length of each wirings 2a, 2b are 13.5 mm. Crosstalks between the wirings 2a and 2b of the multilayered wiring board thus formed were about -40 dB at 1 GHz.

Next, description will be made of the second embodiment of the manufacturing method according to the present invention. In the second embodiment, Steps a-e and Steps h-j are similar to those in the first embodiment. Thus, their description is made only briefly.

(step a)

The surface of the board 3 is polished to provide a mirror finish.

(step b)

A metal film is formed by deposition on the board 3 to form the first wiring layer 1.

(step c)

A resist pattern 11 is formed on the first wiring layer 1.

(step d)

The first wiring layer 1 is subjected to etching to form it into mesh shape.

(step e)

The resist pattern 11 is stripped off.

(step f)

A coating of a non-photosensitive polyimide varnish having the content of a resinous component of 19% is provided on the surface of the first wiring layer 1. Since the content of resinous component is low, it will be depressed, when hardened later, at portions right over the holes 1a formed in the first

wiring layer 1, thus forming an insulating layer 4 having a plurality of recesses.

(step g)

The non-photosensitive polyimide varnish is cured to form an insulating layer 4 of polyimide having a suitable thickness and formed with recesses of suitable depth. Further, though not shown, a resist pattern is formed on the insulating layer 4 by photolithography. The insulating layer is subjected to etching with oxygen plasma to form via holes 12. The resist pattern is of course stripped off.

(step h)

The second wiring layer 2 is formed on the insulating layer 4.

(step i)

A resist pattern 13 is formed on the second wiring layer 2.

(step j)

The second wiring layer 2 is subjected to etching to shape it into a predetermined pattern. Then the resist pattern 13 is stripped off.

Next, description will be made of the third embodiment of the manufacturing method according to the present invention. In the third embodiment, Steps a-e and Steps h-j are similar to those in the first and second embodiments. Thus, their description is made only briefly.

(step a)

The surface of the board 3 is polished to provide a mirror finish.

(step b)

A metal film is formed by deposition on the board 3 to form the first wiring layer 1.

(step c)

A resist pattern 11 is formed on the first wiring layer 1.

(step d)

The first wiring layer 1 is subjected to etching to form it into mesh shape.

(step e)

The resist pattern 11 is stripped off.

(step f)

A coating of a non-photosensitive polyimide varnish having a resinous component content of 50% is provided on the surface of the first wiring layer 1 and the coating is hardened to form a polyimide layer. Since the content of resinous component is high, the surface of the hardened polyimide resin is not depressed but kept flat.

(step g)

Etching treatment is conducted twice.

First, a resist pattern is formed on the polyimide layer so as to cover its entire surface except its portions where it is intended to form via holes 12. Then, etching is performed using oxygen plasma so that the thickness of the polyimide layer is reduced by half at the portions where the via holes 12 are to be formed. The resist pattern is then stripped off.

A resist pattern is again formed on the polyimide layer so as to completely cover its surface except its portions where the via holes 12 are formed and portions right over the holes 1a in the first wiring layer 1. Then, etching is carried out again so as to remove the latter half of the thickness of the polyimide layer at portions where the via holes 12 are formed and thus to completely form the via holes. Further, by this etching treatment, the thickness of the polyimide layer is also reduced by half at portions right over the holes 1a formed in the first wiring layer 1. In other words, the polyimide layer is depressed at portions right over the holes 1a in the first wiring layer 1. Then, the resist pattern is stripped off to complete the insulating layer 4.

(step h)

The second wiring layer 2 is formed on the insulating layer 4

(step i)

A resist pattern 13 is formed on the second wiring layer 2.

(step j)

The second wiring layer 2 is subjected to etching treatment to shape it into a predetermined pattern. Then, the resist pattern 13 is stripped off.

In the embodiments of the manufacturing method according to the present invention, the wiring board is formed by laminating a first wiring layer 1, an insulating layer 4 and a second wiring layer 2, one for each. But, another set of first wiring layer 1, insulating layer 4 and second wiring layer 2 may be formed on the first set of these layers by repeating the above-mentioned steps b - j. Before forming the second set of layers, however, it is necessary to provide an insulating layer on the second wiring layer of the first set and smooth out its top surface. A plurality of such additional sets of layers may be provided. Also, such treatment may be started from any layer in a multilayered wiring board.

In the embodiments, the wiring layers are made of Cu and Cr and the insulating layer is of a polyimide. But they may be made of different materials. For example, the wiring layers may be made of Al and the insulating layer may be of SiO₂ or SiN.

We will now describe another embodiment of the multilayered wiring board according to the present invention.

Fig. 7 is an enlarged perspective view of a portion of the embodiment of the multilayered wiring board. Fig. 8 shows its plan view. Figs. 9(a), 9(b) and 9(c) are sectional views taken along lines A-A, B-B and C-C of Fig. 8.

As will be apparent from these figures, a first wiring layer 21 has a mesh structure with numerous holes formed therein. A second wiring layer 22 comprises a wiring 22a and 22b. On the other hand, the wiring layer 21 is formed on a board 23 of Al₂O₃. An insulating layer 24 is disposed between the first and second wiring layers 21 and 22 (the board 23 and the insulating 24 are shown in Fig. 9). The wiring layer 22 actually comprises numerous wirings. But in the figures, we show only two adjacent wirings.

Each of the wirings 22a and 22b of the second wiring layer 22 extends diagonally over intersections 21b of the mesh pattern of the first wiring layer 21. Between the adjacent intersections 21b, the first wiring layer 21 has protrusions 21a. Thus, as viewed from top, the protrusions 21a are disposed between the adjacent wirings 22a and 22b of the second wiring layer 22 (Fig. 8).

Thus, the distance between each intersection 21b of the mesh pattern of the first wiring layer 21 and the second wiring layer 22 is greater than the distance between any other portion of the first wiring layer 21 and the second wiring layer 22.

In this embodiment, the wirings 22a and 22b of the second wiring layer 22 are arranged at the pitch of 50 microns (each wiring being 25 microns wide, the space therebetween being 25 microns wide). The mesh pattern of the first wiring layer 21

has a diagonal pitch of 100 microns, i.e. twice the pitch of the wirings 22a and 22b. The distance between each intersection 21b of the first wiring layer 21 and the second wiring layer 22 is 6 microns, the protrusions 21a of the first wiring layer 21 being 3 microns high. The second wiring layer 22 has a constant thickness of 5 microns. The wirings 22a and 22b extend in a straight line. The electrical properties of the wiring board of this embodiment concerning crosstalks were measured. The level of crosstalks between the wirings 22a and 22b each 13.5 mm long was about -40 dB at 1 GHz.

In this embodiment, the protrusions 21a of the first wiring layer 21 are 3 microns in height. But their height may be set otherwise within the range of 1 - 10 microns according to the distance between the first and second wiring layers 21 and 22 and the wiring pattern of the second wiring layer 22.

Let us now compare the wiring board of this embodiment with the conventional wiring board shown in Figs. 5 and 6. The wiring board of this embodiment has protrusions 21a formed on the first wiring layer 21 so as to be disposed between the wirings 22a and 22b of the second wiring layer 22 as viewed from top. It is apparent that the conventional wiring board has no such protrusions. Thus, with the wiring board of this embodiment, the electrostatic coupling between first wiring layer 21 and the wirings 22a and 22b is greater than the electrostatic coupling between the wirings 22a and 22b. This means that crosstalks between the wirings 22a and 22b can be reduced to a sufficiently low level by e.g. grounding the first wiring layer and using the wirings 22a and 22b of the second wiring layer 22 as signal transmission lines.

Now, referring to Fig. 10, we will describe another manufacturing method according to the present invention, that is, a method for manufacturing the multilayered wiring board shown in Figs. 7 - 9. In Fig. 10, the protrusions 21a of the first wiring layer 21 and its portions where holes are formed are shown in an exaggerated manner so as to facilitate understanding of the structure.

(step a)

The surface of a board 23 made of Al_2O_3 is polished to provide a mirror finish.

(step b)

A metal film is formed by deposition on the board 23 to form the first wiring layer 21. The metal film has a five-layer structure comprising a 0.1-micron thick Cr film, a 3-micron thick Cu film, a 0.1-micron thick Cr film, a 3-micron thick Cu film

and a 0.1-micron thick Cr film, the total thickness being about 6 microns.

(step c)

A resist pattern 25 that represents the mesh pattern of the first wiring layer 21 is formed by photolithography.

(step d)

The Cr and Cu films forming the first wiring layer 1 are subjected to wet etching using red prussiate and ferric chloride etching solutions to form the upper two metal layers (Cr and Cu layers) into mesh shape.

(step e)

The resist pattern 25 is stripped off.

(step f)

A resist pattern 26 is formed by photolithography to form protrusions 21a on the first wiring layer 21.

(step g)

Wet etching is carried out again to etch the top three of the metal layers formed in Step d.

(step h)

The resist pattern 26 is stripped off to complete the first meshed wiring layer 21 having the protrusions 21a.

(step i)

A non-photosensitive polyimide varnish is applied to the surface of the first wiring layer 21. It was then cured in nitrogen to form a 12-micron thick insulating layer 24.

(step j)

A resist pattern for via holes is formed on the insulating layer 24 and the latter is subjected to dry etching with oxygen plasma using a reactive ion etching apparatus to form via holes 24a in the insulating layer 24.

(step k)

metal film as the second wiring layer 22 is deposited on the insulating layer 24. This metal film has a three-layer structure comprising a 0.1-

micron thick Cr film, a 5-micron thick Cu film and a 0.1-micron thick Cr film.

(step 1)

A wiring pattern is formed in the second wiring layer 22 by photolithography and etching.

On the laminated structure thus formed, the following layers were further laminated one on another in the manner as described above: a polyimide insulating layer; a second wiring layer having a predetermined wiring pattern; a polyimide insulating layer; a first meshed wiring layer; a polyimide insulating layer; and a second wiring layer having a predetermined wiring pattern. A multilayered wiring board having three layers of wiring patterns and two layers of mesh patterns was obtained.

Now referring to Fig. 11, we will describe another embodiment of the multilayered wiring board according to the present invention. In this embodiment, for simplicity of description, we show in Fig. 11 only the section taken along line C-C of Fig. 8. Other sections are omitted.

This embodiment is different from the multilayered wiring board shown in Figs. 7-9 in that it has a layer 27 having protrusions 27a. Also, the first wiring layer 21 is different in sectional shape from that of the embodiment of Figs. 7-9. A first wiring layer 21 having a uniform thickness is laminated on the layer 27. Thus, protrusions 21a is formed on the first wiring layer 21 at portions right over the protrusions 27a. This arrangement of course serves to increase the electrostatic coupling between the wirings of the second wiring layer 22 and the first wiring layer 21, so that crosstalks between the wirings of the second wiring layer 22 can be kept at a low level.

Now referring to Fig. 12, we will describe another method of manufacturing the above-described multilayered wiring board.

(step a)

The surface of a board 23 made of Al_2O_3 is polished to provide a mirror finish.

(step b)

A photosensitive polyimide varnish is applied to the surface of the board 23 with a spinner. Then the board is exposed to light, developed and cured to form a layer 27 having square protrusions 27a arranged in a lattice pattern and having a thickness of 3 microns.

(step c)

A metal film is deposited on the layer 27 by sputtering to form the first wiring layer 21. The metal film has a three-layer structure comprising Cr, Cu and Cr layers, the total thickness being 5 microns.

(step d)

A resist pattern 25 that represents the mesh pattern is formed by photolithography.

(step e)

The Cr and Cu films forming the first wiring layer 21 are subjected to wet etching using red prussiate and ferric chloride etching solutions to form a first wiring layer 21 having a mesh wiring pattern.

(step f)

The resist pattern 25 is stripped off.

(step g)

A non-photosensitive polyimide varnish is applied to the surface of the first wiring layer 21 to form the insulating layer 24.

(step h)

Via holes 24a are formed in the insulating layer 24 by photolithography and etching with oxygen plasma.

(step i)

A metal film is deposited on the insulating layer 24 to form a second wiring layer 22.

(step j)

Resist patterning and wet etching are carried out.

(step k)

The resist pattern is removed to form the second wiring layer 22.

In the embodiments according to the present invention, the wiring layers are made of Cu and Cr while the insulating layers are made of polyimide. But they may be made of any other material. For example, the wiring layers may be made of Al or the insulating layers may be made of SiO_2 or SiN.

Claims

1. A multilayered wiring board having a multilayered wiring structure comprising:
 - a first meshed wiring layer having a plurality of holes formed therein; and a second wiring layer having a plurality of wirings; said wirings of said second wiring layer winding up and down so as to partially sink in said holes formed in said first wiring layer
2. A multilayered wiring board as claimed in claim 1 further comprising an insulating layer provided between said first wiring layer and said second wiring layer; said insulating layer being formed with recesses that are formed so as to partially sink in said holes formed in said first wiring layer; the wirings of said second wiring layer sinking in said recesses in said insulating layer and thus in said holes in said first wiring layer
3. A method for manufacturing a multilayered wiring board comprising:
 - a first step of forming a mesh-shaped first wiring layer having a plurality of holes formed therein
 - a second step of forming an insulating layer on said first wiring layer;
 - a third step of forming recesses in said insulating layer at portions right over said holes formed in said first wiring layer; and
 - a fourth step of forming a second wiring layer comprising a plurality of wirings which partially sink in said recesses in said insulating layer
4. A method for manufacturing a multilayered wiring board as claimed in claim 3; wherein said second step is the step of applying a resin solution which is low in the concentration of resinous component to said first wiring layer to form said insulating layer; and wherein said third step is the step of curing the resin solution applied to said first wiring layer
5. A method for manufacturing a multilayered wiring board as claimed in claim 3; wherein said second step is the step of applying a resin solution which is high in the concentration of resinous component on said first wiring layer and curing said resin solution to form said insulating layer; and wherein said third step is the step of forming recesses in said insulating layer by etching at portions right over the holes in said first wiring layer
6. A method of manufacturing a multilayered wiring board as claimed in claim 3; wherein said insulating layer is formed by applying and curing a polyimide varnish; and wherein said first wiring layer and said second wiring layer are formed of copper or aluminum
7. A multilayered wiring board having a multilayered wiring structure, comprising a first meshed wiring layer having a plurality of holes formed therein; and a second wiring layer having a plurality of wirings; said first wiring layer having a plurality of protrusions protruding into spaces defined between the adjacent ones of said wirings of said second wiring layer
8. A multilayered wiring board as claimed in claim 7 further comprising an insulating layer disposed between said first wiring layer and said second wiring layer
9. A multilayered wiring board as claimed in claim 7 wherein said second wiring layer is flat and has a constant thickness
10. A multilayered wiring board as claimed in claim 7 wherein said first wiring layer is sunk at portions where said protrusions are formed and thin at the other portions
11. A multilayered wiring board as claimed in claim 7 wherein said first wiring layer has a constant thickness even at portions where said protrusions are formed
12. A method for manufacturing a multilayered wiring board, comprising:
 - a first step of forming a first meshed wiring layer having a plurality of holes formed therein;
 - a second step of forming a plurality of protrusions on said first wiring layer by partially reducing the thickness thereof;
 - a third step of forming an insulating layer on said first wiring layer; and
 - a fourth step of forming a second wiring layer on said insulating layer; said second wiring layer comprising a plurality of wirings that extend between said protrusions formed on said first wiring layer
13. A method of manufacturing a multilayered wiring board, comprising:
 - a first step of providing a protrusion-formed layer having a plurality of protrusions;
 - a second step of providing a first wiring layer on said protrusion-formed layer so as to form a plurality of protrusions on said first wiring layer

sions of said protrusion-formed layer.

a third step of providing an insulating layer
on said first wiring layer; and

a fourth step of providing a second wiring
layer comprising a plurality of wirings that ex- 5
tend between said protrusions formed on said
first wiring layer

14. A method for manufacturing a multilayered wir-
ing layer as claimed in claim 12 or 13; wherein 10
said insulating layer is formed by applying and
curing a polyimide varnish; and wherein said
first wiring layer and said second wiring layer
are formed of copper or aluminum.

15

20

25

30

35

40

45

50

55

FIG. 1

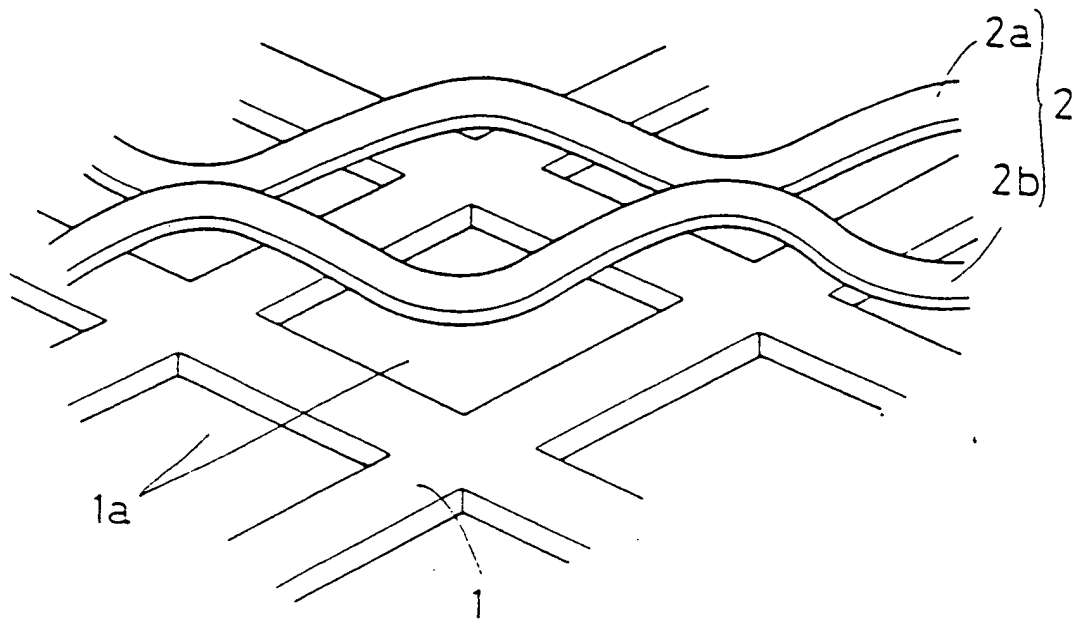


FIG. 2

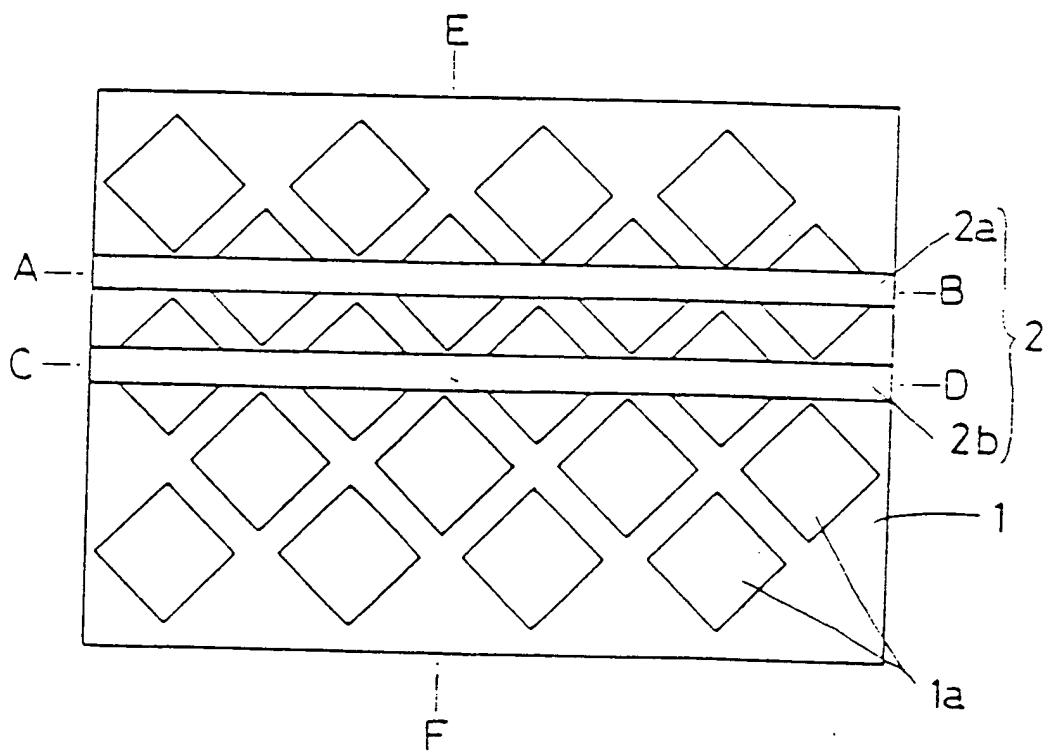


FIG. 3

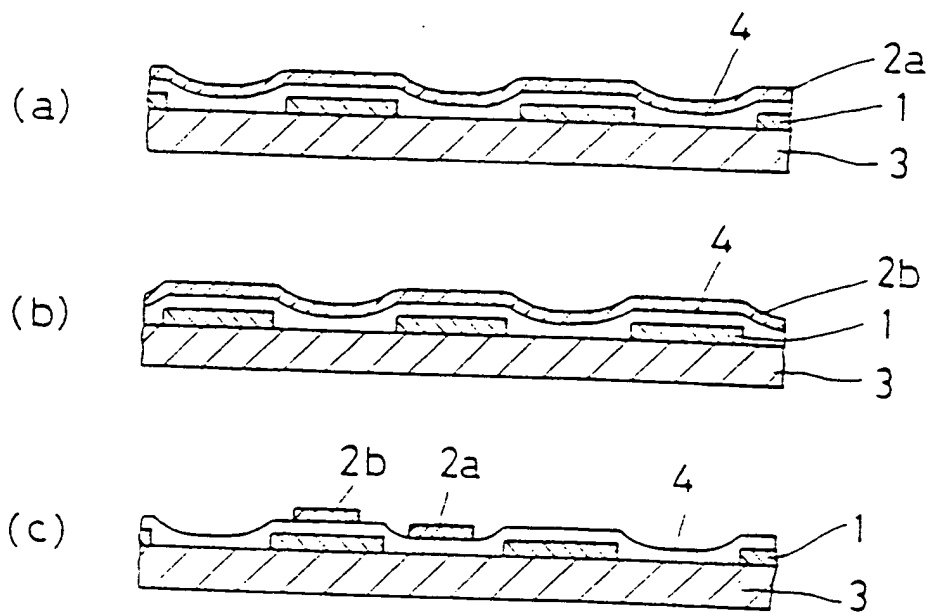


FIG. 5

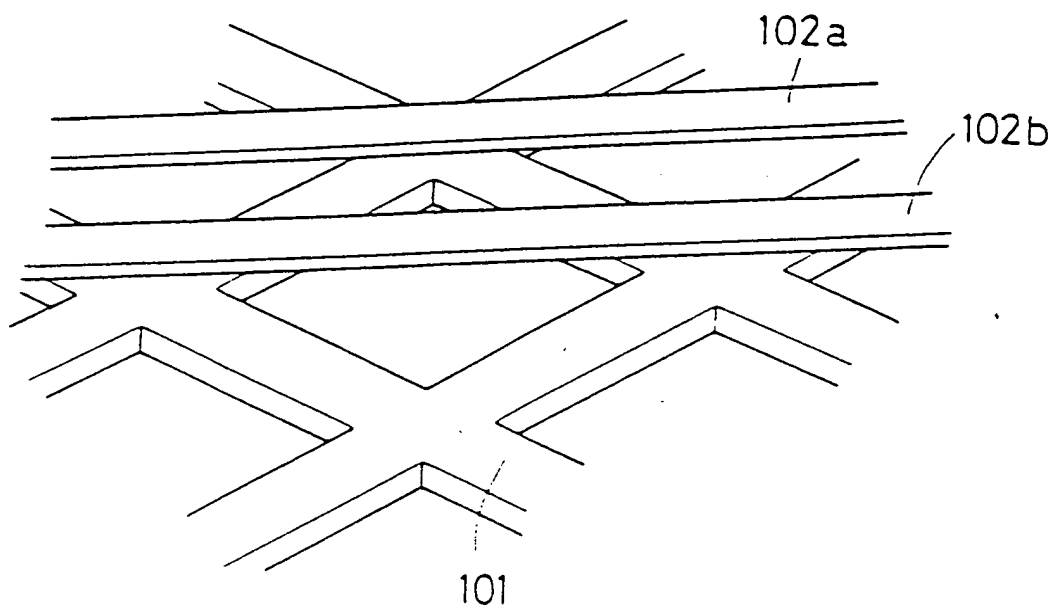


FIG. 6

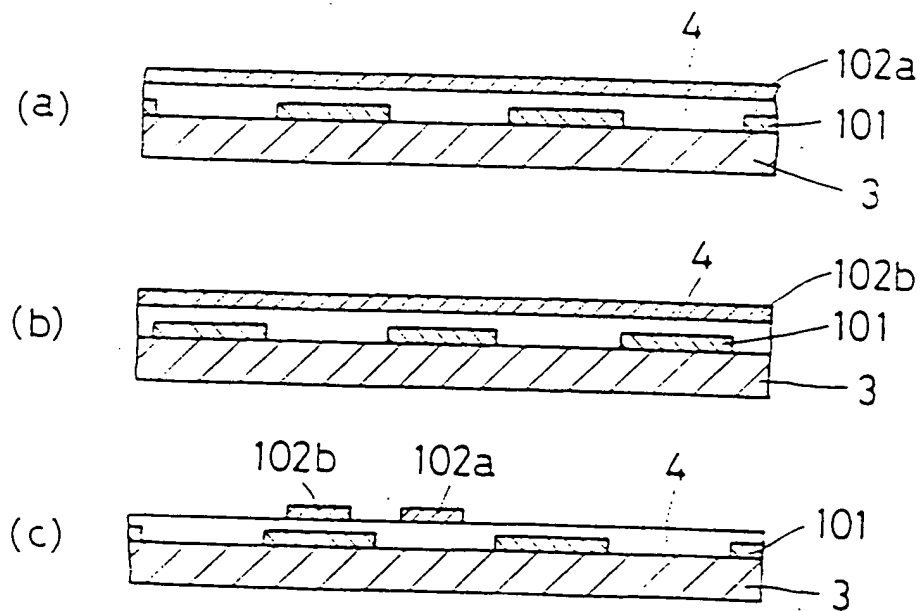


FIG. 7.

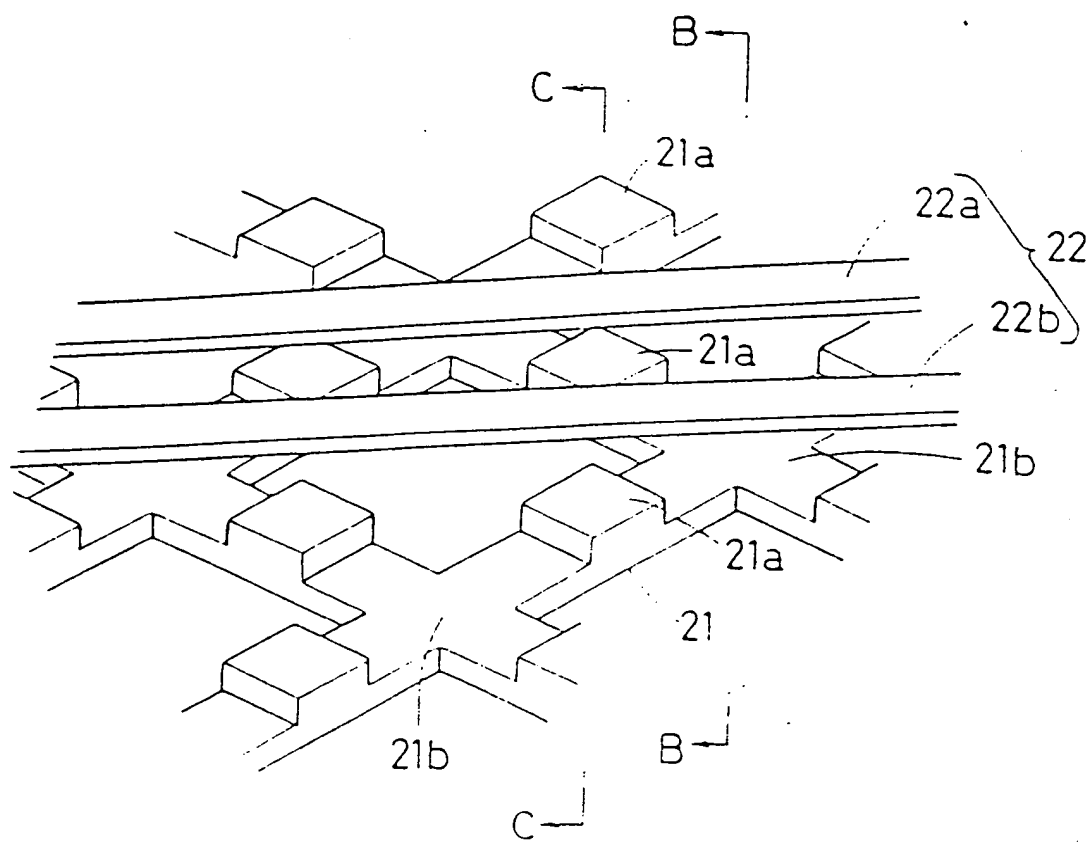


FIG. 8

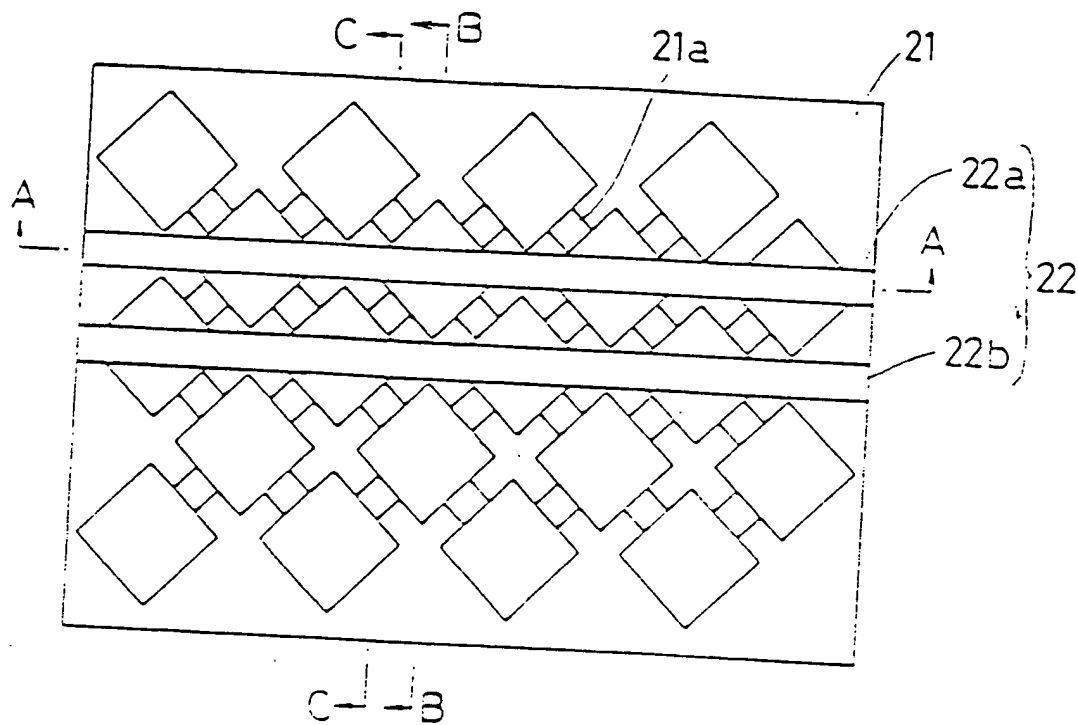


FIG. 9

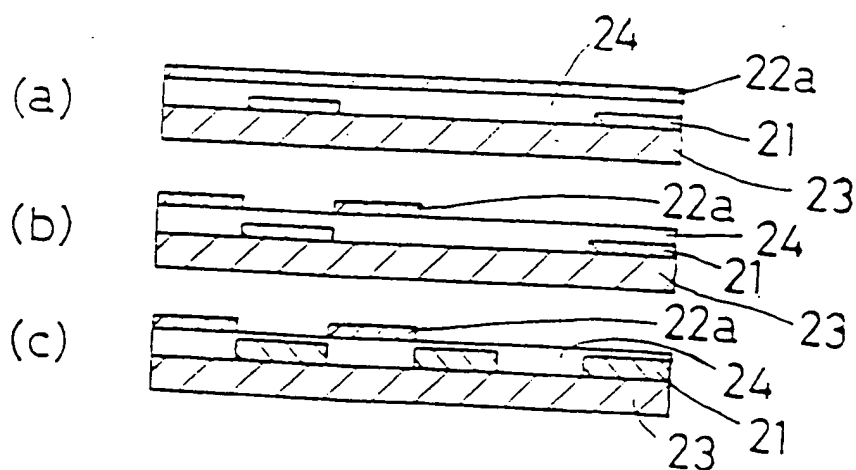
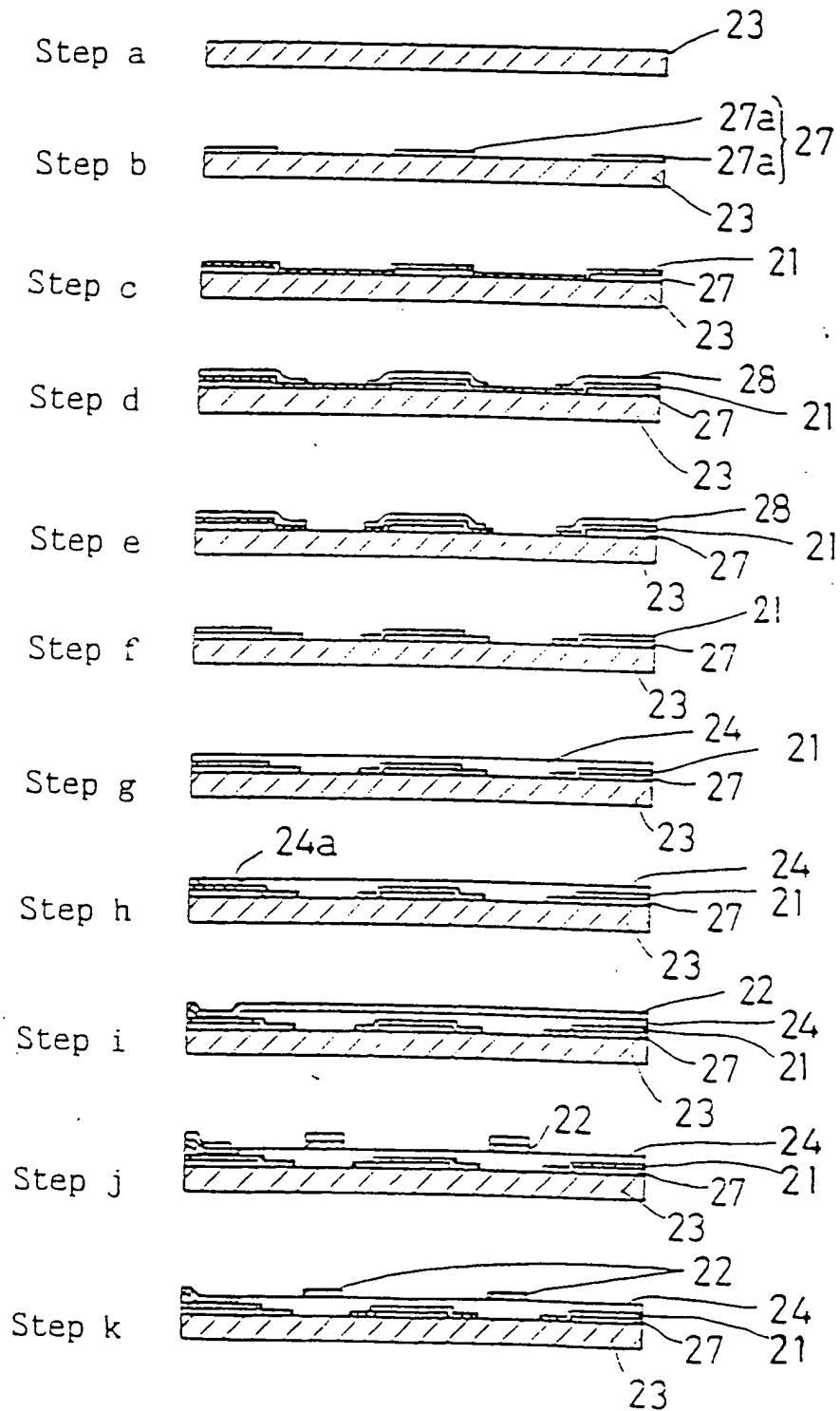


FIG. 12



**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☒ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.